JEDEC STANDARD

Stress-Test-Driven Qualification of Integrated Circuits

JESD47L

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NOTICE

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STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

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(From JEDEC Board Ballot JCB-22-46, formulated under the cognizance of the JC-14.3 Committee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying electronic devices as new products, a product family, or as products in a process which is being changed.

These tests are capable of stimulating and precipitating semiconductor device and packaging failure modes on free-standing devices not soldered to a printed wired board (PWB), or the like (base device reliability). The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure Rate projections usually require larger sample sizes than are called out in qualification testing. For guidance on projecting failure rates, refer to JESD85 Methods for Calculating Failure Rates in Units of FITs.

This qualification standard is aimed at a generic qualification for a range of use conditions, but

- may not be applicable at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments
- does not cover devices assembled onto a PWB, or the like, which may affect the device reliability under assembled state. This is addressed in JEP150 and e.g., typically applies to TC on WLCSP devices

Additional qualification testing tailored to meet specific requirements such as solder joint interconnect reliability can be developed by applying JESD94.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a) Any potential new and unique failure mechanisms.
b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91, “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms” and JESD94, “Application Specific Qualification using Knowledge Based Test Methodology”).

Consideration of PC board assembly-level effects may also be necessary. For guidance on this, refer to JEP150, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.

2 Normative References

The revision of the referenced documents shall be that which is in effect on the date of the qualification plan.

2.1 Military

MIL-STD-883, *Test Methods and Procedures for Microelectronics*.

MIL-PRF 38535, *General Specification for Integrated Circuit Manufacturing*.

2.2 Industrial

UL94, *Tests for Flammability of Plastic Materials for Parts in Devices and Appliances*.

ASTM D2863, *Flammability of Plastic Using the Oxygen Index Method.*

IEC Publication 695, *Fire Hazard Testing.*

J-STD-020, Joint IPC/JEDEC Standard, *Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface-Mount Devices*.

JP-001, *Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites).*

JS-001, *Joint JEDEC/ESDA Standard for Electrical Discharge Sensitivity Test - Human Body Model (HBM) – Component Level*

JS-002, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level*

J-STD-002, *Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires*

JESD22 Series, *Reliability Test Methods for Packaged Devices*

JESD46, *Guidelines for User Notification of Product/process Changes by Semiconductor Suppliers*.

JESD69, *Information Requirements for the Qualification of Silicon Devices*.

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.

JESD78, *IC Latch-Up Test*.

JESD85, *Methods for Calculating Failure Rates in Units of FITs*.

JESD86, *Electrical Parameters Assessment*.

JESD91, *Methods for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JESD94, *Application Specific Qualification using Knowledge Based Test Methodology.*

JEP122, *Failure Mechanisms and Models for Semiconductor Devices*.

JEP143, *Solid State Reliability Assessment Qualification Methodologies.*

JEP150, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.*

JEP156, *Chip-Package interaction Understanding, Identification and Evaluation.*

JESD201, *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes.*

3 General Requirements

3.1 Objective

The objective of this procedure is to ensure that the device to be qualified meets a generally accepted set of stress test driven qualification requirements. Qualification is aimed at devices predominantly used in commercial or industrial operating environments. For other applications, such as automotive, avionics, medical, etc., adjustments to these requirements may be necessary per supplier and customer agreements.

3.2 Qualification Family

While this specification may be used to qualify an individual device, it is designed to also qualify a family of similar devices utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the silicon and package per JEP156 shall be considered in applying family designations.

3.3 Lot Requirements

Test samples shall comprise representative samples from the qualification family. Manufacturing variability and its impact on reliability shall be assessed. Where applicable, the test samples will be composed of approximately equal numbers from at least three (3) non-consecutive lots. Other appropriate means may be used to evaluate manufacturing variability. Sample size and pass/fail requirements are listed in Table 1, Table 2, Table 3, Table 4, Table 5,and Table 6 providing guidance on translating pass/fail requirements to larger sample sizes.

Generic data and larger sample sizes may be employed based upon a Chi Squared distribution using a total percent defective at a 90% confidence limit for the total required lot and sample size. ELFR requirements shall be assessed at a 60% confidence level as shown in Table 4. If a single unique and expensive device is to be qualified, a reduced sample size qualification may be performed using 1/3 the sample size listed in the qualification tables.

3.4 Production Requirements

All test samples shall be fabricated and assembled in the same production site and with the same production process for which the device and qualification family will be manufactured in production. Samples need to be processed through the full production process including burn-in, handling, test, and screening.

3.5 Reusability of Test Samples

Devices that have been used for non-destructive qualification tests may be used to populate other qualification tests. Devices that have been used in destructive qualification tests may not be used in subsequent qualification stresses except for engineering analysis. Non-destructive qualification tests are: Early Life Failure Rate, Electrical Parameters Assessment, External Visual, System Soft Error, and Physical Dimensions.

3.6 Definition of Electrical Test Failure After Stressing

Post-stress electrical failures are defined as those devices not meeting the individual device specification or other criteria specific to the environmental stress. If the cause of failure is due to causes unrelated to the test conditions, the failure shall be discounted.

3.7 Required Stress Tests for Qualification

Table 2, Table 5, and Table 6 list the qualification requirements for new devices. Table 5 and Table 6 are differentiated by package type, but these are not exclusively packaging tests. As outlined in JEP156, interactive effects of the packaging on the silicon also drive the need for tests in Table 5 and Table 6. Power supply voltage for biased reliability stresses should be V_{cc} max or V_{dd} max as defined in the device datasheet as the maximum specified power supply operating voltage, usually the maximum power supply voltage is 5% to 10% higher than the nominal voltage. Some tests such as HTOL may allow for higher voltages to gain additional acceleration of stress time. JEP122 can provide guidance for accelerating common failure mechanisms.

Table 7 lists the stresses that should be considered for a qualification family or category of change. Interactive effects from the unchanged aspects of both the silicon and packaging must be assessed.

3.8 Pass/Fail Criteria

Passing all appropriate qualification tests specified in Table 2, Table 5, and Table 6, either by performing the test, showing equivalent data with a larger sample size, or demonstrating acceptable generic data (using an equivalent total percent defective at a 90% confidence limit for the total required lot and sample size), qualifies the device per this document. When submitting test data from generic products or larger sample sizes to satisfy the Table 2, Table 5, and Table 6 qualification requirements of this document, the number of samples and the total number of defective devices occurring during those tests must satisfy 90% confidence level of a Poisson exponential binomial distribution, as defined in MIL-PRF 38535. MIL-PRF 38535 is available for free from:
http://www.dscc.dla.mil/Programs/MilSpec/listdocs.asp?BasicDoc=MIL-PRF-38535.

The minimum number or samples for a given defect level can be approximated by the formula:

$$N \geq 0.5\,[\chi^2\,(2C+2,\,0.1)]\,[1/LTPD - 0.5] + C$$

where C = accept #, N = Minimum Sample Size, χ^2 is the Chi Squared distribution value for a 90% CL, and LTPD is the desired 90% confidence defect level. Table 1 is based upon this formula, but in some cases the sample sizes are slightly smaller than MIL-PRF-38535.

3.8 Pass/Fail Criteria (cont'd)

Table 1 — Zero Defect Sample Sizes for Stress Tests

			Zero Defect Sampling should be set based on defect type, process maturity and specific application				
			Confidence Level (defect rate)				
Samples per batch	**No. of batches**	**Total Sample**	**40%**	**50%**	**60%**	**75%**	**90%**
77	3	231	≤ 0.2%	≤ 0.3%	≤ 0.4%	≤ 0.6%	**≤ 1.0% ***
45	3	135	≤ 0.4%	≤ 0.5%	≤ 0.7%	**≤ 1.0% ***	≤ 1.7%
30	3	90	≤ 0.6%	≤ 0.8%	**≤ 1.0% ***	≤ 1.5%	≤ 2.6%
25	3	75	≤ 0.7%	**≤ 0.9% ***	≤ 1.2%	≤ 1.8%	≤ 3.1%
15	3	45	**≤ 1.1% ***	≤ 1.5%	≤ 2.0%	≤ 3.1%	≤ 5.1%
* Suggested sampling per confidence level.							

Specific sample plan can be established according to a desired defect rate, and consider the defect type, process maturity and understanding of device application. Agreement between suppliers and customers is recommended.

The confidence levels in Table 1 reflect a zero defect sampling response. For instance, reaching 0 defects for 231 samples would demonstrate ≤1.0% defect rate at 90% confidence level. Conversely, for 0 defects at 90 samples, ≤1.0% defect rate would only carry at 60% confidence.

However, other equivalent defect rates and confidence levels can also be considered using larger sample sizes and non-zero fail counts in accordance with the same non-parametric binomial probability. Refer to Annex B for different sampling plan.

4 Qualification and Requalifications

4.1 Qualification of a New Device

New or redesigned products (die revisions) manufactured in a currently qualified qualification family may be qualified using one (1) wafer/assembly lot. Electrical parameter assessment to accompany each test should be conducted.

4.2 Requalification of a Changed Device

Requalification of a device will be required when the supplier makes a change to the product and/or process that could potentially impact the form, fit, function, quality and/or reliability of the device. A list of changes that may require requalification is shown in clause 6.1.

4.2.1 Process Change Notification

Supplier should follow the guidelines of J-STD-046 "Guidelines for User Notification of Product/Process Changes by Semiconductor Suppliers" for product/process notification changes to consider whether requalification of a device is warranted.

4.2.2 Changes Requiring Requalification

All product/process changes should be evaluated against the guidelines listed in Table 7.

4.2.3 Criteria for Passing Requalification

Table 7 lists qualification plan guidelines for performing the appropriate Table 2, Table 5, and Table 6 stresses. Failed devices should be analyzed for root cause and correction; only a representative sample needs to be analyzed. Acceptable resolution of root cause and successful demonstration of corrective and preventive actions will constitute successful requalification of the device(s) affected by the change. The part and/or the qualification family can be qualified as long as containment of the problem is demonstrated until corrective and preventive actions are in place.

5 Qualification Tests

5.1 General Tests

Test details are given in Table 2, Table 5, and Table 6. Not all tests apply to all devices. Table 2 tests generally apply to design and fabrication process changes. Table 5 tests are for non-hermetic packaged devices, and Table 6 is for hermetic packaged devices. Table 4 lists the pass/fail requirements for common infant mortality levels. Table 7 gives guidance as to which tests are required for a given process change. Some of the data required may be substituted by generic process or package data.

5.2 Device Specific Tests

The following tests must be performed on the specific device to be qualified for all hermetic and plastic packages. Passing or failing these tests qualifies or disqualifies only the device under qualification and not the associated qualification family:

1) Electrostatic Discharge (ESD) - All products. See Table 2.
2) Latch-up (LU) – Required for CMOS, BiCMOS, and Bipolar technologies. See Table 2.
3) Electrical Parameters Assessment - The supplier shall be capable of demonstrating, over the application temperature range, that the part is capable of meeting parametric limits in the individual device specification or data sheet.

5.3 Wearout Reliability Tests

Qualification family testing for the failure mechanisms listed below must be available upon request when a new wafer fabrication technology or a material relevant to the appropriate wearout failure mechanism is to be qualified. JP001 lists requirements for Fabrication Process Qualification. JEP122 explains how to project wearout lifetime for these failure mechanisms. The following mechanisms need to be considered, but there may be other mechanisms to consider based upon technology details.

- Electromigration; EM
- Time-Dependent Dielectric Breakdown; TDDB or Gate Oxide Integrity Test such as Charge to Breakdown.
- Hot Carrier Injection; HCI
- Bias Temperature Instability; BTI
- Stress Migration; SM, may be performed on an actual product.

5.3 Wearout Reliability Tests (cont'd)

The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new device.

5.4 Flammability/Oxygen Index

Certificates of compliance to UL94-0 or ASTM D2863 must be available upon request.

5.5 Device Qualification Requirements

Table 2 — Device Qualification Tests

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	**Duration /Accept**
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$ $V_{cc} \geq V_{cc}$ max	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	$T_J \geq 125°C$ $V_{cc} \geq V_{cc}$ max	See ELFR Table	$48 \leq t \leq 168$ hrs
Low Temperature Operating Life	JESD22-A108	LTOL	$T_J \leq 50°C$ $V_{cc} \geq V_{cc}$ max	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	$T_A \geq 150°C$	3 Lots / 25 units	1000 hrs / 0 Fail
Latch-Up	JESD78	LU	Class I or Class II	1 Lot / 3 units	0 Fail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots / 10 units	T_A per datasheet
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25°C$	3 units	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25°C$	3 units	Classification
Accelerated Soft Error Testing OR System Soft Error Testing	JESD89-2 and JESD89-3 OR JESD89-1	ASER SSER	$T_A = 25°C$	3 units OR Minimum of 1E+06 Device Hrs or 10 fails.	Classification

The Abbreviations column in Table 2 is elaborated upon here:

a) **HTOL** – The duration listed here is generally acceptable to qualify for the given Application Level. However, it does not necessarily imply the demonstration of the lifetime requirement for a particular use condition. It depends on failure mechanisms and application environments. For example, with apparent activation energy of 0.7 eV, 125°C stress temperature and 55°C use temperature, the acceleration factor (Arrhenius equation) is 78.6. This means 1000 hour stress duration is equivalent to 9 years of use. This might be shorter than the application requirement. The equivalent life can be even lower for products or technologies where activation energies are less (e.g., 0.4 eV yields an acceleration factor of ~12 or 1.4 years of equivalent life). In order to assure adequate lifetime requirement, it would be necessary to include Wafer Level Reliability Test information. Wafer Level Reliability can provide information about long term or intrinsic reliability of specific die-level wearout mechanisms, the onset to failure time and design rule (e.g., maximum current density).

5.5 Device Qualification Requirements (cont'd)

For many failure mechanisms, such as dielectric breakdown, elevated voltage will provide additional acceleration and can be used to increase effective device hours or achieve an equivalent life point with a shorter stress duration. Refer to JEP122 for voltage acceleration models. Non-volatile memory devices must be tested for proper operation after HTOL, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

b) **ELFR** – Several methods can be used to calculate the Early Life Failure Rate (ref. JESD74). The objective of ELFR is to measure the failure rate in the first several months or year of operation. Knowledge of the life distribution is generally required to accurately predict ELFR. Equivalently, Table 4 can be used to determine sample sizes to satisfy a particular FPM (cumulative failures) target. Voltage and temperature acceleration may be used to further accelerate effective unit hours. Non-volatile memory devices must be tested for proper operation after ELFR, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

c) **LTOL** – This requirement is aimed at Hot Carrier Degradation and may be satisfied by appropriate wafer level data as specified in JP001. This test is particularly useful when the wafer level data cannot demonstrate adequate life. This test should be run at the maximum frequency of the device with speed parameters data logged. Non-volatile memory devices must be tested for proper operation after LTOL, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

d) **HTSL –** High temperature storage may be accelerated by utilizing a higher temperature; however care must be taken that failure mechanisms are not introduced such as Kirkendall Voiding occurring at very high a temperature or suppressing failure mechanisms such as stress migration at temperatures above 180°C. Alternatively, this test may be performed at the wafer level if packaged device reliability has been addressed with generic data. Non-volatile memory devices must be tested for proper operation after HTSL, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

e) **LU** – Verify V_{cc} overvoltage and I/O trigger current resistance to latch-up per JESD78.

f) **ED** – This study is to be performed on key device parameters; it is not aimed at all datasheet parameters.

g) **ESD-HBM** – Classification of Human body Model ESD sensitivity.

h) **ESD-CDM** – Classification of Charge Device model ESD sensitivity.

i) **ASER** – Accelerated alpha particle and beam soft error testing may be utilized together to project the field soft error rate. For parts without B^{10} in the process, the only beam soft error testing required is high energy neutron or proton soft error testing; thermal neutron soft error beam testing is not required for such parts. This test is required for devices with a significant portion of the circuit utilizing volatile memory elements or latches. Generic data taken on products or test devices with similar memory elements or latches and equivalent critical charge may be substituted.

j) **SSER** – System soft error testing requires enough device hours to be accumulated to produce 10 failures or at least 1E6 device hours must be accumulated. High altitude testing may be used to accelerate this stress. This test may be utilized in lieu of or in addition to accelerated soft error testing. Generic data taken on products or test devices with similar memory elements or latches and equivalent critical charge may be substituted.

5.5 Device Qualification Requirements (cont'd)

Table 3 — Additional Qualification Tests for Non-volatile Memory Device

Stress	Ref.	Abbv.	Conditions		Requirements	
					# Lots/SS per lot	**Duration / Accept**
Non-volatile Memory Uncycled High Temperature Data Retention	JESD22-A117	UCHTDR	FG-CT	$T_A \geq 125°C$	3 Lots/ 77 units	1000 hrs / 0 Fail[(a)]
			PCM	$T_A \geq 90°C$		
Non-volatile Memory Cycling Endurance	JESD22-A117	NVCE	25 °C and $85°C \geq T_J \geq 55°C$		3 Lots / 77 units	Up to Spec. Max Cycles[(b)] / 0 Fails
Non-volatile Memory Post-cycling High Temperature Data Retention	JESD22-A117	PCHTDR	FG-CT	Option 1: $T_J = 100°C$	3 Lots/ 39 units	Cycles per NVCE (≥55°C) / 96 and 1000 hrs / 0 Fail[(c)]
				Option 2: $T_J \geq 125°C$		
			PCM	Option 1: $T_J = 90°C$		Cycles per NVCE (≥55°C) / 10 and 100 hrs / 0 Fail[(c)]
				Option 2: $T_J \geq 100°C$		
Non-volatile Memory Low-Temperature Data Retention and Read Disturb	JESD22-A117	LTDDR	$T_A = 25°C$		3 Lots / 38 units	Cycles per NVCE (25°C) / 500 hrs / 0 Fail[(d)]
NOTE FG-CT are intended to denote Floating Gate and Charge Trapping memories whereas PCM denotes Phase Change memories.						

The abbreviations in Table 3 are elaborated upon here:

a) **UCHTDR –** Uncycled non-volatile memories data retention failure mechanisms are generally accelerated by temperature and are modeled using the Arrhenius Equation for acceleration. The duration listed is generally acceptable for qualification but do not necessarily demonstrate the retention requirement for a particular use condition, which depends on failure mechanisms, acceleration factors and application environment. If the application requirement does not match the UCHTDR test's retention values then a knowledge-based qualification should be followed (see JESD94). For devices specified to have some non-zero bit error rate, bit errors may not be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117).

5.5 Device Qualification Requirements (cont'd)

b) **NVCE** – Figure 1 describes the flow for NVCE, PCHTDR and LTDDR. 38 units are cycled at room temperature and 39 units are cycled at elevated temperature.

Quantity of Cycling: Cycling should be performed to the max spec. cycle count on 50% of cells and to 10% of max spec. cycle count on the other 50% of cells when this is possible within 500 hours. For large memories where this is not possible, the total program/erase operations are to be the number possible in 500 hours. This will be accomplished by reducing the fraction of cells cycled to max spec. and increasing the fraction cycled to 10% of max spec. In some cases it will be necessary to cycle some fraction of cells to less than 10% of max spec. to ensure that all cells receive some cycling, excluding any limited number of uncycled sectors which are used as a reference for post-cycling comparison. At least one-third of the operations should be devoted to cycling blocks to 100% of maximum specification, if possible, within the specified cycling time frame. For multi-block memories, at least one block of each device must be cycled to the max. spec. cycle count, regardless of the time required. Such cycling conditions are generally acceptable also for system implementing wear leveling; otherwise, a knowledge based qualification can be implemented.

Delays and Cycling Rate: The supplier may specify that cycling not exceed a certain rate per day or that delays or bakes be inserted between cycles, to avoid overstress due to unrealistic conditions or to emulate delays expected in intended application. Consider these five constraints:

1. The quantity of cycling is for 500 hours of actual cycling operations, not counting inserted delays.
2. Inserted delays must be distributed per the guideline in JESD22-A117.
3. For room-temperature cycling, no high-temperature delays are to be inserted.
4. For high-temperature cycling, the delays plus the cycling time itself must not add up to more than 500 hours at 85°C (longer delays acceptable at lower temperatures per JESD22-A117, 4.1.2.4).
5. If the cycling activation energy is significantly lower than 1.1eV, cycling temperatures higher than 85°C are allowed, with a strong technical justification consistent with JESD94.

These delays do not necessarily demonstrate the effect that would be seen with a particular use condition. For example, with apparent activation energy of 1.1 eV for dielectric charge detrapping, the delay durations are equivalent to 1.5 years of cycling at 55°C. An application condition with less delay would be more severe than is represented by the qualification delays specified above. If application use conditions deviate considerably from the cycle counts or equivalent times described above, then an application-specific qualification methodology can be pursued per JESD94. For devices operated with Bad Block Management and specified to have a non-zero bad-block rate, a unit with blocks failing program/erase is to be counted as a failure if the number of such blocks exceeds the allowed bad-block specification (see JESD22-A117, 2.5). For devices specified to have some non-zero bit read error rate, bit errors are not to be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117, 2.8, and 5.2).

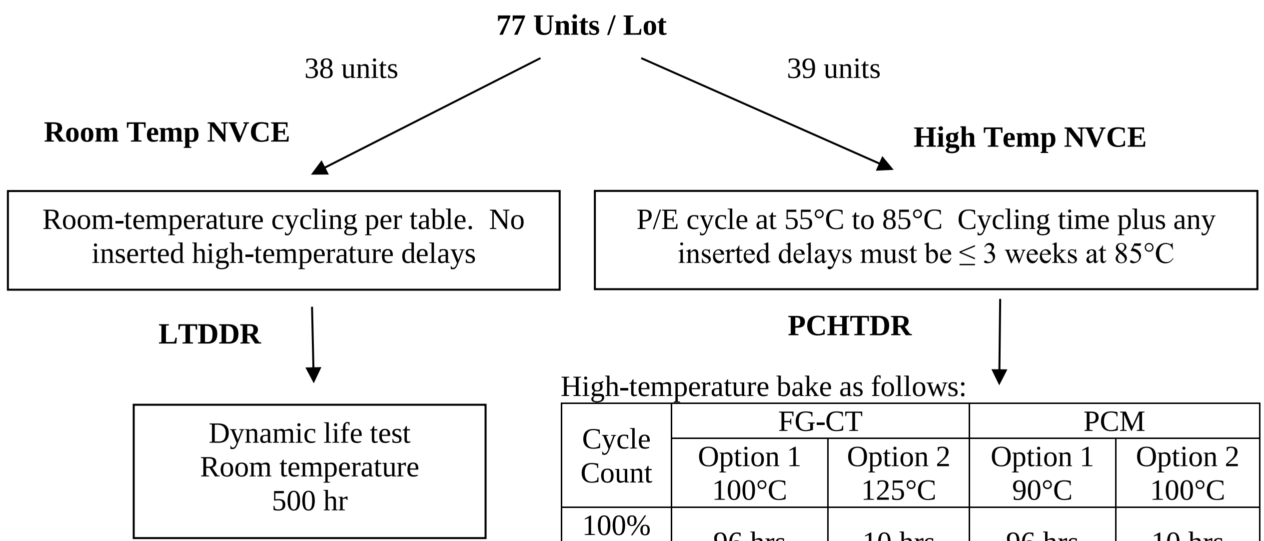
c) **High Temp NVCE + PCHTDR** – Figure 1 describes the flow for PCHTDR. Units sent through High Temperature NVCE are placed in high-temperature retention bake. Two options are given, either of which is acceptable for qualification, and for each option, there are two bake durations. The longer of the two durations is to be applied to the blocks cycled to ≤ 10% of the max. spec. cycles. The shorter of the two is to be applied to blocks cycled to 100% of max. spec. cycles. For example option 2 requires that blocks cycled to ≤ 10% of max. spec. cycles retain data for 100 hours of 125°C (FG-CT) / 100°C (PCM) bake, and blocks cycled to 100% of max. spec. cycles must retain data for 10 hours of 125°C (FG-CT) / 100°C (PCM) bake. The durations listed are generally acceptable for qualification but do not necessarily demonstrate the retention requirement for a particular use condition, which depends on failure mechanisms and application environments.

5.5 Device Qualification Requirements (cont'd)

For example, with activation energy of 1.1 eV for dielectric For example, with activation energy of 1.1 eV for dielectric charge detrapping, 125°C stress temperature (option 2) and 55°C use temperature, the acceleration factor (Arrhenius equation) is 939.

Bake time is then equivalent to 11.3 years for 10% of max. spec. cycles and 1.1 years for 100% of max. spec. Retention lifetime necessary in use will be less than total product lifetime, because the PCHTDR requirement is a sequential reliability stress that is preceded by up to one lifetime's worth of endurance cycling (NVCE). If the application requirement does not match these retention values, or the technology has different activation energy, then a knowledge-based qualification should be followed (see JESD94). For devices specified to have some non-zero bit error rate, bit errors may not be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117).

d) **Room Temp NVCE + LTDDR** – Figure 1 describes the flow for LTDDR. Units sent through Room Temperature NVCE are placed into room-temperature operating-life stress which sequentially performs dynamic read accesses on all memory addresses. 25°C stress temperature is used to determine sensitivity to non-temperature-accelerated retention failure mechanisms, or to mechanisms that can entirely recover at high temperatures, such as the SILC mechanism. Biased life stress is performed to detect voltage-induced disturbs due to random bit accesses, in addition to unbiased data retention mechanisms which occur when a bit is not being accessed. Inserted bakes as described for NVCE are not acceptable for the 25°C cycling condition used prior to LTDDR. If the cycle counts from note (b) or the retention lifetimes of 500 hours are insufficient to meet a specific application requirement, or if bit accesses in application are expected to be highly concentrated on specific bits, then knowledge-based qualification methods using special techniques should be used (see JESD94). Note that at the end of the NVCE + LTDDR test, data retention must be verified. For devices specified to have some non-zero bit error rate, bit errors may not be counted towards device failure but must be shown to meet the bit error rate specification (see JESD22-A117).



Cycle Count	FG-CT		PCM	
	Option 1 100°C	Option 2 125°C	Option 1 90°C	Option 2 100°C
100% spec	96 hrs	10 hrs	96 hrs	10 hrs
10% spec	1,000 hrs	100 hrs	1,000 hrs	100 hrs
< 10% spec	1,000 hrs	100 hrs	1,000 hrs	100 hrs

Figure 1 — NVCE / PCHTDR / LTDDR

5.5 Device Qualification Requirements (cont'd)

Table 4 — Minimum Sample Size to Demonstrate Various ELFR Targets in FPM (Failures per Million) at 60% Confidence Level

Number of observed failures	Equivalent failures at 60% Confidence Level ($\chi^2/2$)	Minimum sample sizes required to meet FPM target at 60% confidence level					
		4000 FPM	2000 FPM	1000 FPM	500 FPM	250 FPM	100 FPM
0	0.92	229	458	916	1,833	3,665	9,163
1	2.02	505	1,011	2,022	4,045	8,089	20,223
2	3.11	778	1,553	3,105	6,211	12,422	31,054
3	4.18	1,004	2,088	4,175	8,351	16,701	41,753
4	5.24	1,310	2,618	5,237	10,473	20,946	52,366
5	6.29	1,573	3,146	6,292	12,584	25,168	62,919
6	7.34	1,835	3,671	7,343	14,685	29,371	73,426
7	8.39	2,098	4,195	8,390	16,780	33,559	83,898
8	9.43	2,358	4,717	9,434	18,868	37,736	94,340
9	10.48	2,620	5,238	10,476	20,951	41,903	104,757
10	11.52	2,800	5,758	11,515	23,031	46,061	115,153

5.6 Non-hermetic Package Qualification Test Requirements

Table 5 — Qualification Tests for Devices in Non-hermetic Packages

Stress	Ref.	Abbv	Conditions	Requirements	
				# Lots / SS per lot	**Duration / Accept**
MSL Preconditioning Must be performed prior to: THB, HAST,TC, AC, & UHAST	JESD22 - A113	PC	Per appropriate MSL level per J-STD-020		Electrical Test (optional)
High Temperature Storage[1]	JESD22-A103 & A113	HTSL	150°C + Preconditioning if Required	3 Lots / 25 units	1,000 hrs / 0 Fail
Temperature[2] Humidity bias (standard 85/85)	JESD22-A101	THB	85°C, 85% RH, V_{cc} max	3 Lots / 25 units	1,000 hrs / 0 Fail
Temperature[2, 3] Humidity Bias (Highly Accelerated Temperature and Humidity Stress)	JESD22-A110	HAST	130°C / 110°C, 85% RH, V_{cc} max	3 Lots / 25 units	96 / 264 hours or equivalent per package construction / 0 Fail
Temperature Cycling	JESD22-A104	TC	B[4] -55°C to +125°C	3 Lots / 25 units	700 cyc / 0 Fail
			G[4] -40°C to +125°C		850 cyc / 0 Fail
			C[4] -65°C to +150°C		500 cyc / 0 Fail
			K[4] 0°C to +125°C		1,500 cyc / 0 Fail
			J[4] 0°C to +100°C		2,300 cyc / 0 Fail
Unbiased Temperature/Humidity (Unbiased HAST[3])	JESD22-A118	UHAST	130°C / 85% RH 110°C / 85% RH	3 Lots / 25 units	96 hrs / 0 Fail 264 hrs / 0 Fail
Unbiased Temperature / Humidity (Autoclave[5])	JESD22-A102	AC	121°C / 100% RH	3 Lots / 25 units	96 hrs / 0 Fail **Not Recommended**
Solder Ball Shear	JESD22-B117	SBS	Characterization	30 balls / 5 units	
Wire Bond Pull[7]	JESD22-B120	BPS	Characterization, Pre Encapsulation	1 Lot / 30 bonds / 5 units	Ppk ≥ 1.66 or Cpk≥1.33 (note 6)
Bond Shear[7]	JESD22-B116	BS	Characterization, Pre Encapsulation	1 Lot / 30 bonds / 5 units	Ppk ≥ 1.66 or Cpk≥1.33 (note 6)
Solderability	M2003 J-STD-002	SD	Characterization	3 lots / 22 leads	0 Fail
Tin Whisker Acceptance	JESD22-A121 through rqmts of JESD201	WSR	Characterization per JESD201	See JESD201	See JESD201, Based on Appropriate Classification

Table 5 — Qualification Tests for Devices in Non-hermetic Packages (cont'd)

NOTE 1 Preconditioning to JESD22-A113 is recommended, specifically for wire-bonded products qualified to Pb-free reflow profiles. Moisture soak as part of the preconditioning is optional.

NOTE 2 Either HAST or THB may be chosen.

NOTE 3 If THB or HAST is run, then UHAST need not be run.

NOTE 4 It is recommended that the Temperature Cycling condition is chosen applying the following criteria:

- Condition *G, B or C* may not be appropriate unless the device will be subjected to a sub 0 °C cycle in its routine field operating life.
- Condition *G, B or C* may not be appropriate for Flip Chip packages with organic substrates.
- The condition chosen should encompass the range that device will be subjected to in its routine field operating life.
- Annex A explains the failure mechanisms and models used for the choice of temperature cycling conditions. Refer to JEP122 for reliability models and JESD94 for application-specific test method when selecting a different test condition or defining a different test duration. Selection should correspond to a targeted failure mechanism and reconcile with application and use condition if possible because stress test durations can be quite different depending on the coefficient value (n).
- Any Temperature Cycling condition specified in JESD22-A104 may be used following the methodology in Annex A. Different conditions may be established per supplier and customer agreement.

NOTE 5 Autoclave is not recommended as a qualification test; Unbiased or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave.

NOTE 6 Ppk = $\frac{\bar{x} - LSL}{3\sigma}, \frac{USL - \bar{x}}{3\sigma} \geq 1.66$. Process capability data may be substituted for Ppk with data on more than 30 lots with the requirement that $Cpk \geq 1.33$.

NOTE 7 See 7.1 for Bond Shear and 7.3 for Wire Bond Pull failure criteria.

The Conditions column in Table 5 is elaborated upon here:

a) **HTSL** This test is basically used to determine if the effects of diffusion, oxidation, intermetallic growth, and chemical degradation of packaging devices will affect product life.

b) **THB** will accelerate the three basic corrosion models: Galvanic, Electrochemical and direct Chemical. It will also accelerate ion migration. Must be run at minimum power dissipation.

c) **HAST** is a test used to accelerate the THB test. Must be run at minimum power dissipation. It is suggested that 130°C for 96 hours be used for leaded devices and 110°C for 264 hours be used for Ball Grid Arrays.

d) **TC** will accelerate damage caused by thermal-mechanical stress as a result of thermal mismatch and dimensional differences.

e) **UHAST** is the preferred technique to test for Galvanic and direct Chemical corrosion.

f) **AC (Autoclave)** is the less desirable alternative to UHAST testing. It can introduce condensation and pressure induced mechanical damage that are not representative of package field life stresses. Autoclave is not recommended for organic substrate packages.

g) **PC (Pre-Conditioning)** ensures that a device will be able to withstand multiple assembly cycles, and to simulate the stress from Printed Circuit Board assembly that a device in a field operation would receive prior to acceleration stress testing.

h) **SBS (Solder Ball Shear)** ensures that the BGA balls have the desired shear strength attachment to the package.

5.6 Non-hermetic Package Qualification Test Requirements (cont'd)

i) **BPS (Bond Pull Strength)** ensures that wire bond exhibits the desired tensile strength. See 7.3 for failure criteria.

j) **BS (Bond Shear)** ensures that the wire ball bond exhibits the desired shear strength. See 7.1 for failure criteria.

k) **SD (Solderability)** ensures that the device leads are capable of being wetted by the board attachment solder.

l) **WSR (Tin Whisker Susceptibility)** for use when tin (Sn) or tin alloy surface finishes are used. This acceptance procedure provides a basis for comparison between surface finishes with respect to the propensity for whisker growth, but does not provide a basis for prediction of whisker growth in field use conditions.

5.7 Hermetic Package Qualification Tests

These packages are typically used in long term applications and severe environments so some requirements may be different than for non-hermetic packages.

Table 6 — Qualification Test for Devices in Hermetic Packages

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	Duration / Accept
Temperature Cycling	JESD22-A104	TC	-55°C to +125°C or alternatives with temperature justification	3 Lots / 25 units	700 cycles / 0 Fail
Wire Bond Pull[3,4]	JESD22-B120	BPS	Characterization	1 lot / 30 bonds / 5 units	Ppk ≥ 1.66 or Cpk ≥ 1.33
Bond Shear [3,4]	JESD22-B116	BS	Characterization	1 lot / 30 bonds / 5 units	Ppk ≥ 1.66 or Cpk ≥ 1.33
Solderability	M2003 J-STD-002	SD	Characterization	3 lots / 22 leads	0
Solderball Shear	JESD22-B117	SBS	Characterization	5 units	10 balls per unit
Mechanical Shock[1]	JESD22-B104 M2002	MS	Y1 plane only, 5 pulses, 0.5 ms duration, 1,500 g peak acceleration	3 lots / 39 units	TEST after CA
Vibration Variable Frequency[1]	JESD22-B103 M2007	VVF	20 Hz to 2 kHz (log variation) in > 4 minutes, 4X in each orientation, 50g peak acceleration	Sequence from MS	TEST after CA
Constant Acceleration[1]	M2001	CA	Y1 plane only, 30 kg force < 40 pin packages, 20 kg for ≥ 40 pins.	Sequence from VVF	Test at room temp. pre & post –stress
Gross / Fine Leak	JESD22-A109 M1014	GFL	Any fine test followed by gross test. May also be performed at the beginning of the mechanical sequence before mechanical shock test.		
External Visual		EV			1
Physical Dimensions		PD		1 lot / 30 units	2
Lead Integrity		LI		45 leads; min of 5 units	1
Lid Torque		LT		1 lot / 5 units	1
Internal Water Vapor	MIL-STD 883 M1018	IWVC	Residual Gas Analysis of Package Cavity Water Vapor Content	3 lots / 1 unit ea.	Characterization
Tin Whisker Acceptance	JESD22-A121	WSR	Characterization per JESD201	See JESD201	See JESD201, Based on Appropriate Classification

NOTE 1 Based upon manufacturer specification or applicable procurement documents.
NOTE 2 Reference applicable JEDEC spec, supplier specification, or procurement document for significant dimensions and tolerances.

NOTE 3 $Ppk = \frac{\bar{x} - LSL}{3\sigma}, \frac{USL - \bar{x}}{3\sigma} \geq 1.66$. Process capability data may be substituted for Ppk with data on more than 30 lots with the requirement that $Cpk \geq 1.33$.

NOTE 4 See 7.1 for Bond Shear and 7.3 for Wire Bond Pull failure criteria.

5.8 Additional Device Information

Any additional information (e.g., device construction, materials, manufacturing locations, etc.) should be reported in accordance with JESD69 Information Requirements for the Qualification of Silicon Devices.

6 Explanatory Comments Regarding Process / Product Changes

6.1 Typical Changes That Require Re-qualification to be in Compliance with J-STD-046

Active Circuit Element: New type of circuit element or modification of transistors beyond original qualification or spec limits.

Major Circuit Elements: Addition of a major new circuit block to an existing circuit such as adding a Digital Signal Processor or embedded memory block to an existing product.

Wafer Diameter Change

Metallization: New Materials or a significant change in composition

Change In Minimum Feature Size: A reduction of greater than 20% shall be considered a new process.

Wafer Fab Process: Utilizing different process techniques at critical points (excluding wafer transport equipment)

Diffusion/Dopant: New material or technique

Polysilicon or other MOSFET gate material: Composition, design rules, process

Lithography: Change in wavelength, method (air / immersion / e-beam), or etch technique

Wafer Frontside Metallization: Composition, design rules, process and/or technique

VIA: Composition, design rules, process and/or technique

Passivation Overcoat: Either glass or organic material composition, design rules, process and/or technique

Dielectric Materials: Composition, design rules, process and/or technique

Low-K Dielectric: A dielectric material used for inter-metal isolation with a K value less than 3.2.

Wafer Backside Operation: Metal composition, design rules, process and/or technique

New Wafer Manufacturing Line: Not already qualified for the fabrication process

Assembly Process: Utilizing different process techniques at critical points

Die Coating: Material, process, and/or technique

Lead Frame: Base material, finish, and critical dimensions

Bond Wire: Material, diameter

Bonding: Process and/or technique

Die Preparation: Separation and clean methods

Die Attach: Material, process, and/or technique

Encapsulation: Material, composition, process and/or technique

6.1 Typical Changes That Require Re-qualification (cont'd)

Hermetic Package: Material, composition, seal material, process and/or technique

Wafer Bumping Material: Process, or technique (including flip chip assembly process)

Package Dimension Change: Larger package body size or reduction in lead or solder ball pitch.

Die Thickness

New Chip-Package Combination

6.2 Changes That May Not Require Re-qualification

Previously qualified foundries or assembly locations: Unless the previously qualified facility, or packages/products from said facility, have been dormant, suspended or discontinued for a period longer than three years.

The addition of previously qualified equipment: Requires completion of process capability study only, to assure that the added equipment delivers an adequate process distribution.

A change to a test program or test equipment: Requires proof of continued conformance to product specification only.

Any change in a process, product or material parameter: That does not exceed the current specified production process range is not a major change.

Minor changes to device logic operation: May only require functional verification.

Smaller package or die: Where the product family has already been qualified.

6.3 Multiple Family Qualifications

When the specific product attribute to be qualified will affect more than one wafer fab or assembly family, the qualification test vehicles should be:

1) One lot of a single device type from each of the three (3) products that are projected to be most sensitive to the changed attribute, or
2) Three lots total from the most sensitive families if only one or two exist.

The following is the recommended process for qualifying changes across many process and product families:

1) Identify all products affected by the proposed changes.
2) Identify the critical structures and interfaces potentially affected by the proposed change.
3) Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Note that steps 1 to 3 are equivalent to the creation of an FMEA.
4) Define the product groupings or families based upon similar characteristics as they relate to the structures and device sensitivities to be evaluated, and provide technical justification for these groupings.

6.3 Multiple Family Qualifications (cont'd)

5) Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products that will address each of the potential failure mechanisms and associated failure modes including any justifiable generic family data.
6) Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process steps.

6.4 Guidelines for Stress Tests for Product / Process Changes

Table 7 lists the recommended (R) qualification tests for each type of change in the process, package, or device design, and additional tests that should be considered (C) based upon technology considerations.

Table 7 — Guidance for Selection of Tests Per Product / Process Changes

Process Attribute	HTOL	ELFR	LTOL	HTSL	NVCE+DR	LU	ED	ESD-HBM	ESD-CDM	ASER	THB/HAST	TC	UHAST	BPS	BS	SD	SBS	MS	VVF	CA	GFL	LI	LT	EM	HC	BTI	TDDB
Active Circuit Element	C		C																						R	R	
Major Circuit Change	R		C			C	C	C	C																		
5% to 20% Die Shrink	R	R	C	C		R	R	R	R	R	R	C												C	R	R	
Lithography	C		C				R																		C	C	
Doping	C					C		C																	R	R	
Polysilicon	C				R							R													R	R	C
Metallization	C	C		R							C	R	C											R			
Gate Oxide	R	C	C		R		C																		R	R	R
Interlayer Dielectric Non-Low-K	C	C		C								C												R			C
Low-K Dielectric	R	C		R							R	R												R			C
Passivation	C	C			C						C	C	R														
Contact	C	C		R	C																			R			
Via	C	C		R																				R			
Bump Site				R						a)			R														
Wafer Diameter	R		C	C	R			C	C		C	R	C											R	R	R	R
Wafer Bump Materials or Process				C						a)		R	R														
Wafer Bump Under-Metal				R						a)		C	R														
Wafer Saw Technique												C	C														
Fab Site	R			R							C	R	C														
New Package to Qualified Product	C			C					C		C	R	R	R	R	R	R	R	R	R	R	R	C				
Leadframe Plating[1]																R						C					
Leadframe Material												C				R			C	C		R					
Package Dimensions, including Trace Pitch												C	C				C		C	C	C	C					
Wire Bonding				R							C	R	C	R	R			C	C								
Multi-Chip Module Die Separation												R	C														
Die Attach												R	C					C	C	C							
Die Thickness	C				C							R	R														
Molding Compound	C			R							R	R															
Package Substrate Material											C	R					R	C	C	C							
Package Substrate Plating											C			R			R										
Molding Process				C								R	C														
Flip Chip Attach Method				C							R	R															
Flip Chip Underfill										a)		R	R														
Assembly Site											R	R		R	R	R	R	C	C	C	C	C	C				
Burn-in Elimination		R																									
Burn-in Reduction[b)]		C																									

R – Recommended
C – Consider

a) - Measure material alpha emissivity.
b) - May be based upon defect density reduction with justification.

NOTE 1 Additional consideration may be necessary when evaluating product changes with respect to tin whiskers. Consult JESD201 when making changes involving high tin content materials. A separate table is located in JESD201 that addresses whisker test requirements based on various types of changes.

7 Wire Bond Qualification Requirements

7.1 Failure Criteria for Wire Bond Shear Test Method (JESD22-B116) for Unencapsulated and Unstressed Bonds

The following failure criteria are intended to be applied as a production monitor of the wire bonding process as well as for qualification and process development. They are not valid for devices that have undergone environmental stress testing, have been desoldered from circuit boards, or were preconditioned (some procurement or qualification documents require that the samples be preconditioned prior to the performing of this test method).

Refer to 4.6 in JESD22-B116 for guidance on acceptable and non-acceptable fail modes.

7.1.1 Shear Failure Criteria for Gold and Copper Ball Bonds on Aluminum Bond Pads

The following equation is applicable for "gold" and "copper" wire ball bonds on aluminum alloy bond pads. "Gold" wire includes doped gold wire. "Copper" wire includes palladium coated copper, palladium coated copper with gold flash, and doped copper wires. The determination of whether a shear value is acceptable is determined by using this equation:

$$\text{Measured\_shear\_force\_value} \div \text{ball\_bond\_area} \geq 0.0062\ \text{gf}/\mu\text{m}^2$$

The above shear failure criterion shall be applied to all copper ball bonds on aluminum bond pads. This criterion shall also be applied to all new device qualifications with gold ball bonds on aluminum bond pads. Previously qualified devices with gold ball bonds on aluminum bond pads may either meet the above criterion or the previous criterion stated in Table 5-1 of JESD-B116A (August 2009).

If alternate units of force or area are used for this test, the value of 0.0062 gf/μm^2 shall be replaced with one of the following appropriate conversions: 61 N/mm^2 or 4.0 gf/mil^2.

Alternate minimum bond shear values may be proposed by the supplier if supporting data justifies the proposed minimum values and the customer agrees.

Other material combinations (wire and/or bonding surface) may require a new set of failure criteria.

7.1.2 Shear Failure Criteria for Gold and Copper Ball Bonds on Copper Base Metal Bonding Surfaces

At the time of the most recent revision of this document there was not enough data available to propose a value for acceptable shear force for gold or copper ball bonds on copper base metal bonding surfaces.

7.2 Failure Criteria for Wire Bond Shear Test Method (JESD22-B116) for Encapsulated and Stressed Bonds

There is too much variability between device construction, decapsulation processes, and stress conditions for this document to propose failure criteria for the shearing of ball bonds that have been decapsulated or have been exposed to production or qualification stresses.

7.3 Failure Criteria for Wire Bond Pull Test Method (JESD22-B120) for Unencapsulated and Unstressed Bonds

The following failure criteria are intended to be applied as a production monitor of the wire bonding process as well as for qualification and process development for gold (Au), copper (Cu), and aluminum (Al) unencapsulated wire bonds. They are not valid for devices that have been encapsulated (e.g., overmolded, hermetically sealed, etc.) or have been stressed (e.g., preconditioned, thermal cycled, etc.).

The determination of whether a pull value is acceptable is determined by using Table 8. Refer to JESD22 B120 clause 5.5, for assigning fail codes and clause 5.5.2 for guidance on acceptability of fail codes.

Table 8 — Minimum Pull Values for Au, Cu, and Al Bonds (Unencapsulated)

Wire Diameter			**Minimum bond strength** (grams force) (unencapsulated) **Au & Cu**	**Minimum bond strength** (grams force) (unencapsulated) **Al**
microns (controlling)	mils (conversion)	mils (rounded)		
15	0.59	0.6	1.7	Out of scope
18	0.71	0.7	2.0	1.5
20	0.79	0.8	2.3	1.8
23	0.91	0.9	2.6	2.1
25	0.98	[a]	2.9	2.3
25.4	1.0	1.0	3.0	2.5
30	1.18	1.2	3.6	(N/A)
32	1.26	1.25	(N/A)	3.0
33	1.30	1.3	4.0	(N/A)
38	1.50	1.5	5.0	4.0
43	1.69	1.7	5.9	4.8
50	1.97	2.0	7.5	6.0
65	2.55	2.6	10	7.8
75	2.95	3.0	15	12
100	3.94	4.0	22	17
125	4.92	5.0	36	27
150	5.91	6.0	50	40
200	7.87	8.0	85	60
250	9.84	10	125	95
300	11.8	12	170	130
380	15.0	15	240	190
500	19.7	20	350	280
600	23.6	24	460	360
[a] Left blank on purpose				

At the time of the most recent revision of this document there was not enough data available to propose minimum pull values for silver wire bonds.

7.3 Failure Criteria for Wire Bond Pull Test Method (cont'd)

For wire diameters not listed in Table 6, determine the minimum pull value using the graph in Figure 2, which is Figure 2011-2 in Mil-Std 883, Method 2011.9. Curve 1 is to be used for unencapsulated Au & Cu wire and Curve 2 for unencapsulated Al wire.

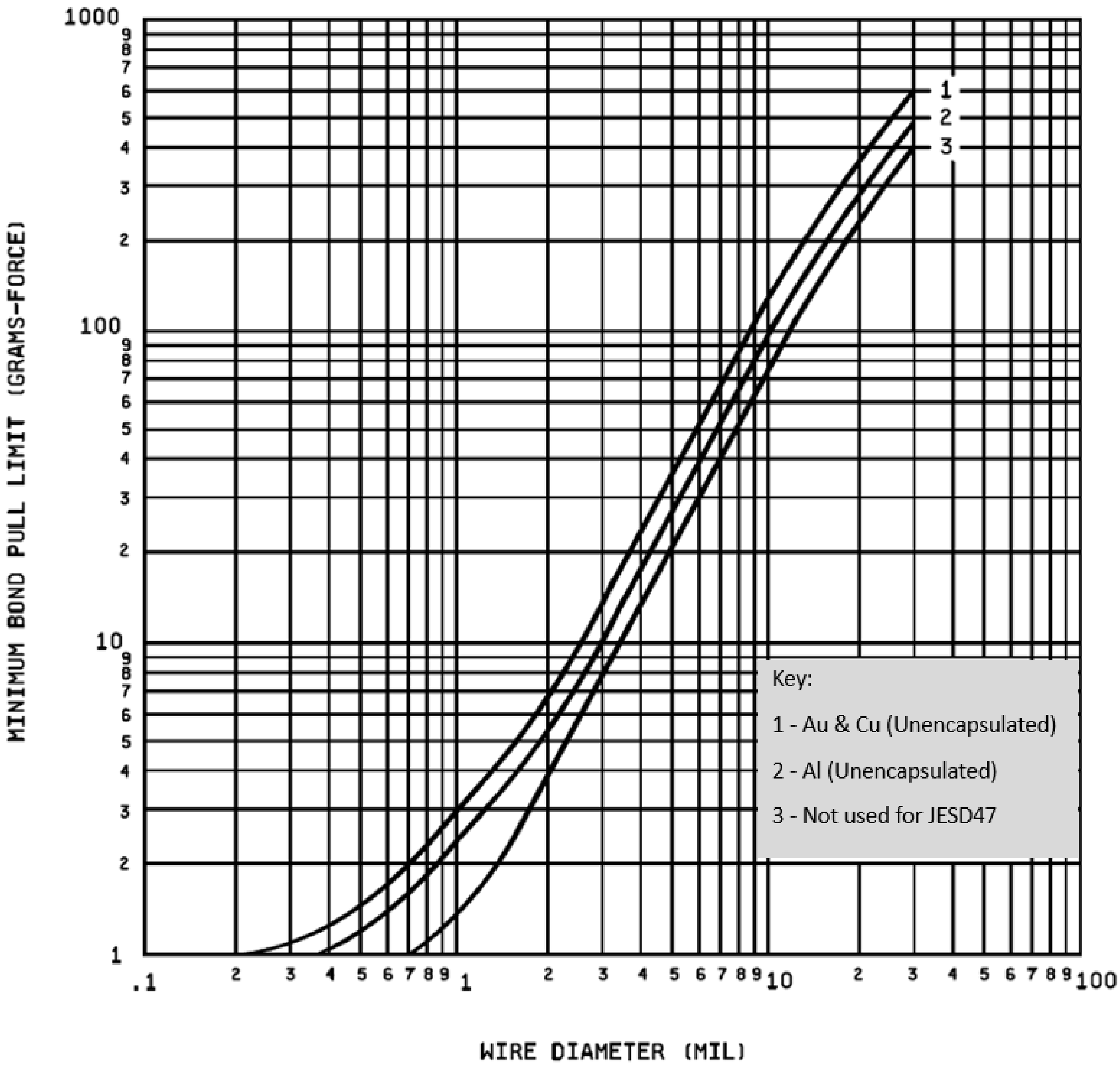


Figure 2 — Minimum Bond Pull Limits

7.4 Failure Criteria for Wire Bond Pull Test Method (JESD22-B120) for Encapsulated and Stressed Bonds

At this time JESD47 does not require wire bond pull testing of devices post-encapsulation or post-stress. Refer to Mil-Std 883 Method 2011 for the minimum pull values for wires in devices post-encapsulation and post-stress.

Annex A (Informative) Non-hermetic Package Temperature Cycling Variations for Solder Joint

Solder joint Reliability is generally the limiting factor for device life in a system subjected to temperature cycling. Solder joint life is well modeled by a Coffin-Manson relation of ΔT^n where n = 2 (e.g., board level / SMT attach – solder joint fatigue). Other failure mechanisms as reported in JEP122 have larger acceleration factors so this is considered a worst case condition. The temperature cycling requirements have been normalized to the historical requirement of 500 cycles of Condition C using the n = 2 factor. As a sanity check the typical use conditions for a number of common applications have been compared to these qualification conditions. As can been seen in the Table 9, the qualification requirements exceed the use conditions by a wide margin.

Table 9 — Non-hermetic Package Temperature Cycling Variations

Use Condition	Use Condition Requirement	Equivalent Condition B -55°C to +125°C 700 cycles	Equivalent Condition G -40°C to +125°C 850 cycles	Equivalent Condition J 0°C to +100°C 2300 cycles
Desktop 5 yr life	ΔT 40°C 2,000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15°C 1,500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr life	ΔT 40°C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr life	ΔT 25°C 5,500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr life	ΔT 6°C 5,500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year life	ΔT 30°C 3,000 cy	25,200 cy	25,712 cy	25,557 cy

[a)] JESD94, Table 5-1, Consider Desktop with additional ΔT 8°C for 31,025 cycles and ΔT 20°C for 1,828 cycles.

[b)] Consider Desktop with additional ΔT 10°C for 50,000 cycles.

Annex B (Informative) Sampling Options with Non-zero Failures

Table 10 provides a list of sampling plans with varying Lot Tolerance Percent Defect (LTPD) and defect quantity. Each column value – LTPD – corresponds to a demonstrate defect rate that is achieved when the defect does not exceed the acceptance number.

For instance, setting qualification requirements of LTPD = 1, then for a sampling of n = 230, 0 rejects would be permitted. Conversely, if 668 samples were tested, then to achieve LTPD = 1, the corresponding maximum number of rejects would be 3 assuming that failures were equally distributed (based on consecutive sampling).

Table 10 — Sample Size for a Maximum % Defective at a 90% Confidence Level

Acceptance Number	LTPD	LTPD	LTPD	LTPD	LTPD	LTPD	LTPD
C	**10**	**7**	**5**	**3**	**2**	**1.5**	**1**
0	22	32	45	76	114	153	230
1	38	55	77	129	194	259	389
2	53	76	106	177	266	355	532
3	67	96	134	223	334	446	668
4	80	115	160	267	400	533	800
5	94	133	186	310	465	619	928
6	107	152	212	352	528	703	1054
7	119	170	237	394	590	786	1179
8	132	188	262	435	652	868	1301
9	144	205	287	476	713	949	1423
10	157	223	311	516	773	1030	1543
11	169	240	335	556	833	1110	1663
12	181	258	359	596	893	1189	1782

Annex C (Informative) Differences Between Revisions

Summary of changes made to entries that appear in this standard, JESD47L, compared to its predecessor, JESD47K (August 2018).

Differences Between JESD47L and JESD47K

Clause	Description of Change
Document	In all instances where appropriate, replaced the term "component" with "device." Tables and Figures were re-numbered (Tables are sequentially re-numbered 1 through 10, Figures are 1 through 2).
Table 5	Changed reference from Mil-Std 883 Method 2011 to JESD22-B120 for Wire Bond Pull and updated Note 7 to align with title of B120
Table 6	Changed reference from Mil-Std 883 Method 2011 to JESD22-B120 for Wire Bond Pull and updated Note 4 to align with title of B120
7.3	Modified title of this clause. Removed the reference to Mil-Std 883 Method 2011 and all accompanying text. Added reference to JESD22-B120, *Wire Bond Pull Test Methods*, along with accompanying text and Table 8 - Minimum pull values for Au, Cu, and Al bonds (unencapsulated)
7.4	Added new clause, "Failure criteria for wire bond pull test method (JESD22-B120) for encapsulated and stressed bonds," which points the user to Mil-Std 883 Method 2011

Differences Between JESD47K and JESD47J.01

Clause	Description of Change
1, 3.1	Scope clarification for potential tailoring of requirements based on device application and use condition.
2.1, 2.2	Update references (MIL-PRF-38535, JESD91, JEP156)
3, 5, 6	Re-numbering Tables for consistency (Table A to Table 3-1, Table 1 to 5-1, Table 1a to Table 5-1a, Table B to Table 5-2, Table 2 to Table 5-3, Table 3 to Table 5-4 and Table 4 to Table 6-1)
3.6	Temperature considerations for electrical testing post stress test
3.2, 3.7	Reference to JEP156
3.8	Table 3-1 clarification and usage
4.2, 4.2.1	Requalification consideration
5.2	Replacement of organic package
5.5	Clarification for HTOL example (eV, acceleration factor impact) and HTSL (defect occurrence)
Table 5-1	Clarification on JESD89-1 or JESD89-2 and JESD89-3 test selection
Table 5-1a	Alignment for FG-CT and PCM options with Figure 1 flowchart and update LTDDR
5.5 b), c)	Improve readability for descriptive test steps
5.5 d)	Update to LTDDR (Low Temperature Data Retention and Read Disturb) per Figure 1
5.6	Typesetting correction (NOTE) per revised JEDEC manuals and clarification on selection of stress test condition
5.8	Expanding clause – previously omitted
Table 6-1	Title clarification
6.1, 6.2	Alignment with 4.2, 4.2.1 – requalification considerations (J-STD-046 and other changes)
6.3	Generic data use
Annex A	Clarification on CM parameter (solder joint fatigue)
Annex B	New, for legacy purposes, the Sampling table (previously listed as Table 3-1)

Differences between JESD47J.01 and JESD47J (August 2017)

Clause	Description of Change
7.1.1	2nd paragraph, changed equation to "(measured shear force value ball bond area) ≥ 0.0062 gf/□m2"

Differences between JESD47J and JESD47I.01 (October 2016)

Clause	Description of Change
5.6	In Table 5-3 modified sample requirement for wire pull and bond shear to be from 1 Lot which now matches requirement in Table 5-4. Added Footnote 7 which states that failure criteria for bond pull strength and bond shear are in new subclauses 7.3 and 7.1 respectively
5.7	Added Footnote 4 which states that failure criteria for bond pull strength and bond shear are in subclauses 7.3 and 7.1 respectively
6.4	Added "C" (Consider) for THB/HAST stress for Wire Bonding
7	Added new clause 7, "Wire bond qualification requirements". Subclause 7.1 states the failure criteria for the bond shear test for both gold and copper ball bonds on aluminum bond pads. Subclause 7.2 provides guidance for performing shear testing on bonds that have been encapsulated or stressed. Subclause 7.3 provides guidance regarding the failure criteria for the wire pull test method.

Differences between JESD47I.01 and JESD47I (July 2012)

Clause	Description of Change
2.2	Added JS-001, JS-002, and J-STD-002 to References. Removed JESD22-A121 specific reference.
5.5	Table 5-1 CDM spec reference changed to JS-002 from JESD22-C101
5.5	Changed "resistance" to "sensitivity" in notes g) and h)
5.6	Table 5-3 Solderability spec reference changed to J-STD-002 from JESD22-B102
5.7	Table 5-4 Solderability spec reference changed to J-STD-002 from JESD22-B102

Differences between JESD47I and JESD47H.01 (April 2011)

Clause	Description of Change
1	Added material to 2nd and 5th paragraph and removed material in Scope
5.5	add last sentence to a), b), c), and d)
Figure 1	Added details for PCM
Global	changed Ta to T_A and changed Tj to T_J

Differences between JESD47H.01 and JESD47H

Clause	Description of Change
Table 5-1	Updated Human Body Model reference from JESD22A-114 to JS-001

Differences between JESD47H and JESD47G.01

Clause	Description of Change
Table 5-1	001Updated Latchup requirements to align with latest revision of JESD78

Differences between JESD47G.01 and JESD47G

Clause	Description of Change
Table 5-1	Under latch-up changed Conditions, from T_A = 25°C and Tj max to Class I or Class II.
5.5(h)	Added “per JESD78” to end of sentence.

Differences Between JESD47G and JESD47F

Page	Description of Change
7	In Table 5-1, NVCE, change temperature range to 85°C $\geq T_J \geq$ 55°C and add fail criteria (0 fails)
7	In Table 5-1, LTDR, change reference document to JESD22-A117
7	In Table 5-1, NVCE, HTDR and LTDR entries, add number of Note.
8	Note (e): Specify fraction of device that needs to be cycled 100%, 10% and less than 10% of endurance spec. Specify constrains for delays between cycles
9	Note (e): In definition of failure, add consideration of Bad Block management and allowed bit-error rate.
9	Note (f), (g): In definition of failure, add consideration of allowed bit-error rate
10	Figure: Set NVCE temperature range to 85°C $\geq T_J \geq$ 55°C, remove table redundant to Note (e),

Differences Between JESD47F and JESD47E

2.2	Added references, JESD201 and JESD22A121
5.6	Table 5-3; added “Tin Whisker Acceptance” row
5.7	Table 5-4; added “Tin Whisker Acceptance” row
6.4	Table 6-1; under “New package to Qualified Product”, changed ESD-HBM from “R” to blank (no requirements) and ESD-CDM from “R” to “C”. Added reference 1 below table

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The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:
   - ☐ Requirement, clause number ________
   - ☐ Test method number ________ Clause number ________

   The referenced clause number has proven to be:
   - ☐ Unclear ☐ Too Rigid ☐ In Error
   - ☐ Other ________________________________

2. Recommendations for correction:

   ____
   ____
   ____
   ____

3. Other suggestions for document improvement:

   ____
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